

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Prior Application: Y. SASAKI et al
Serial No. 08/930,219
Filed: October 20, 1997

Group Art Unit: 2763
Examiner: H. Jones
For: METHOD FOR DESIGNING SEMICONDUCTOR
INTEGRATED CIRCUIT AND AUTOMATIC
DESIGNING DEVICE



CLAIM FOR PRIORITY

Commissioner of Patents
Washington, D.C. 20231

Sir:

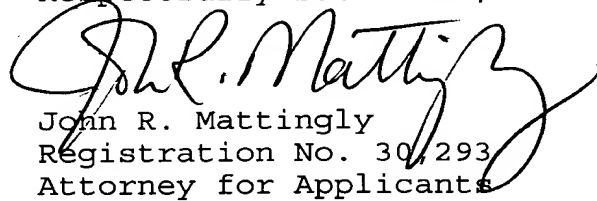
Applicants claim priority under 35 U.S.C. §120 of U.S. Serial No. 08/930,219, filed October 20, 1997, U.S. Serial No. 08/633,486, filed April 17, 1996 and foreign priority under 35 U.S.C. §119 of Japanese Application No. JP 7-96487 filed April 21, 1995; and

Applicants further claim priority under 35 U.S.C. §120 of U.S. Serial No. 08/633,053 filed on April 16, 1996 and priority under 35 U.S.C. §119 of Japan Patent Application No. JP 7-99204, filed April 25, 1995; and

Applicants claim priority of International Application PCT/JP96/01104 filed on April 24, 1996 claiming priority of Japanese Application No. JP 7-99204.

Applicants do not submit copies of the certified priority documents of the above-identified Japanese applications since the certified copies of these documents have been filed in the respective U.S. applications.

Respectfully submitted,


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